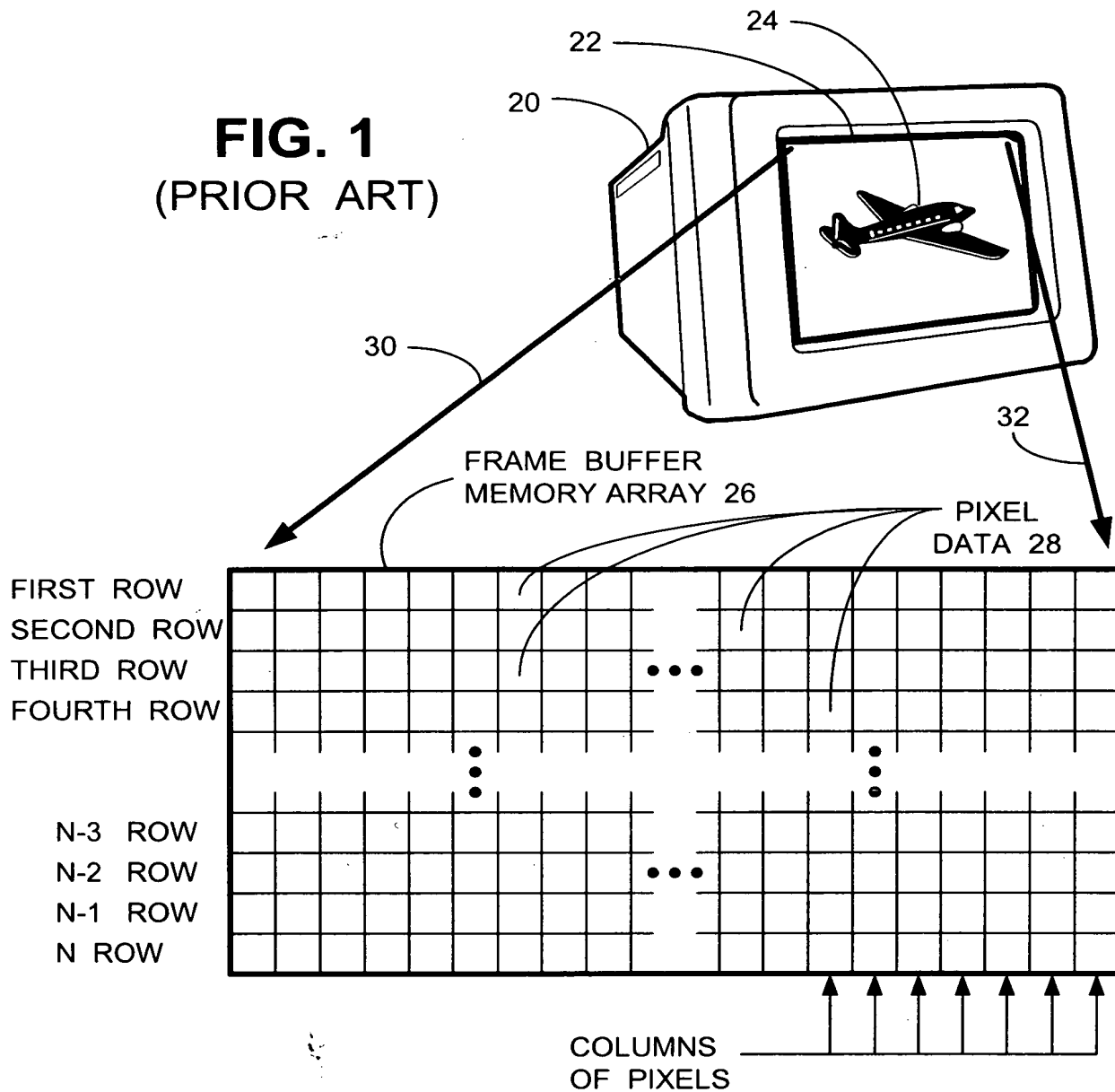
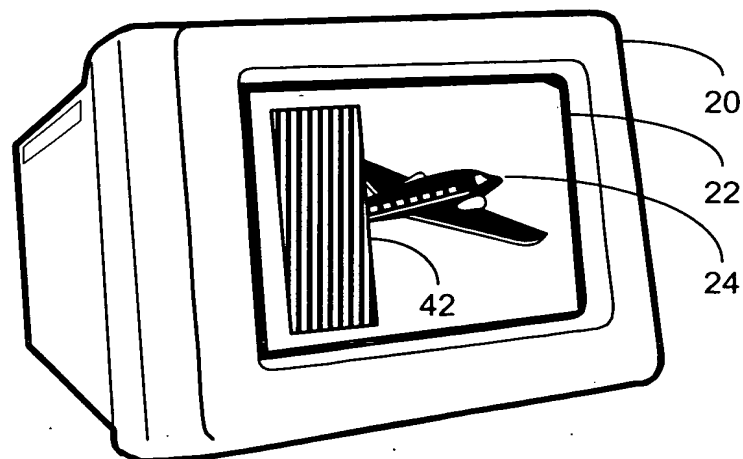


**FIG. 1**  
(PRIOR ART)



**FIG. 2**  
(PRIOR ART)



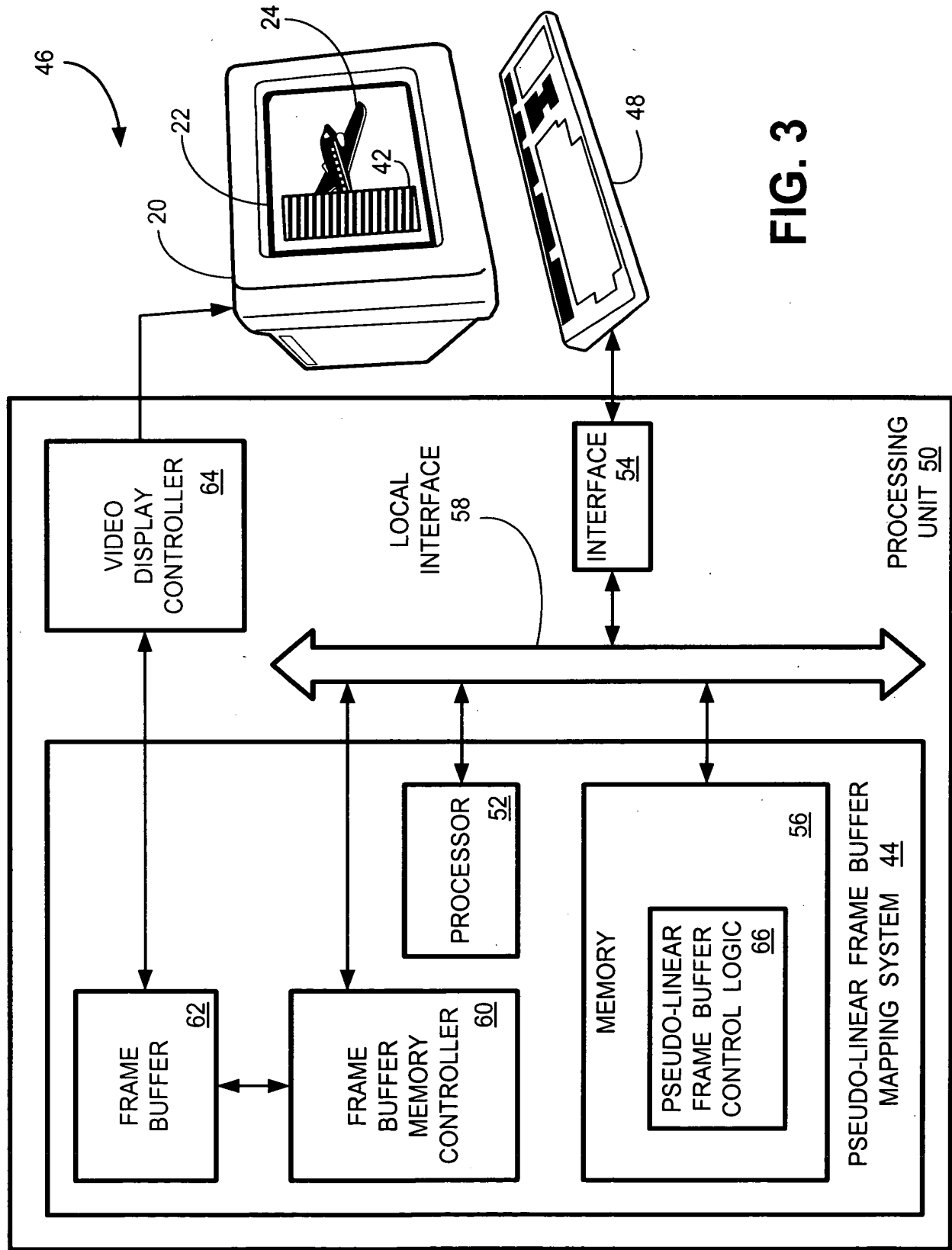


FIG. 3

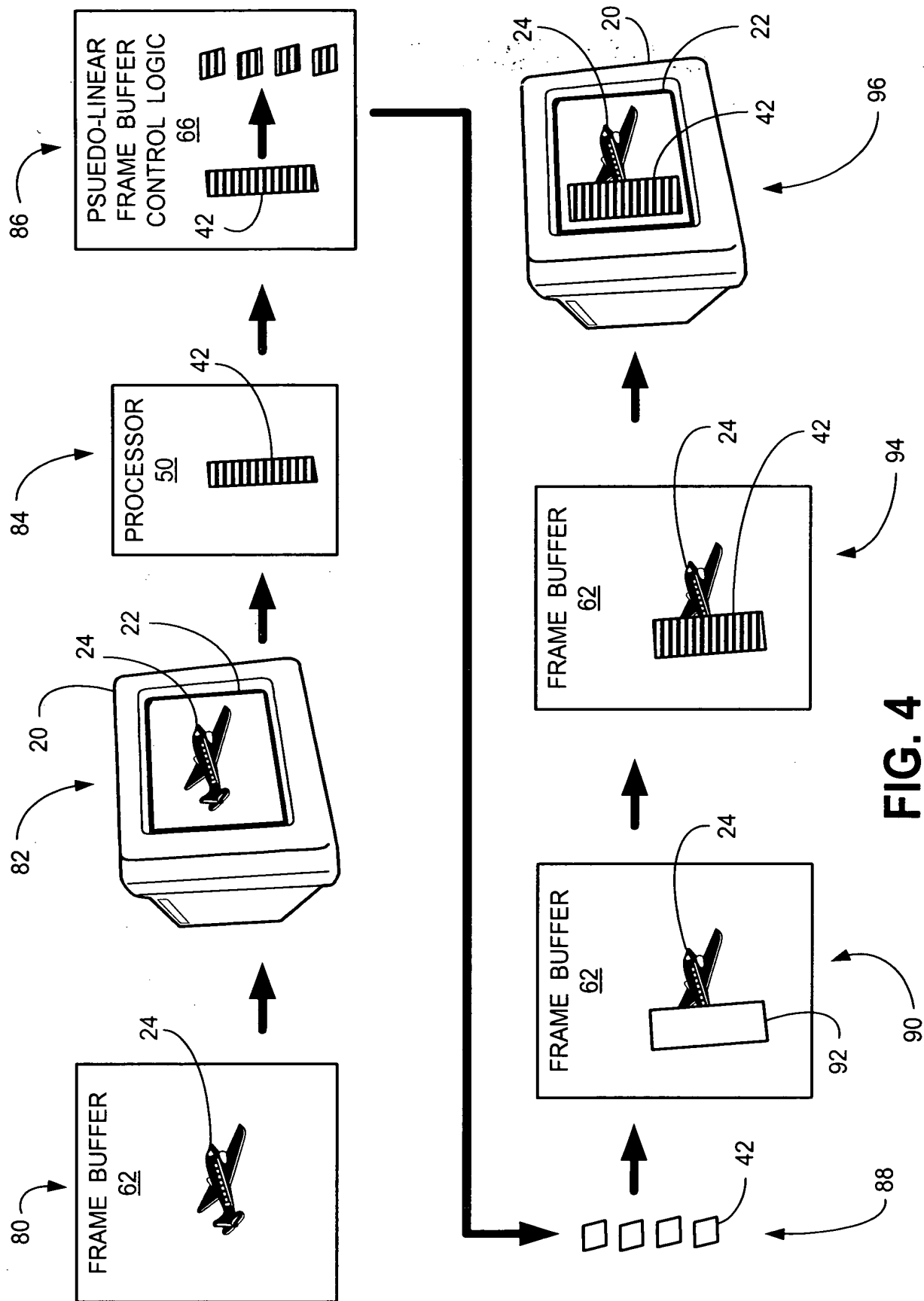
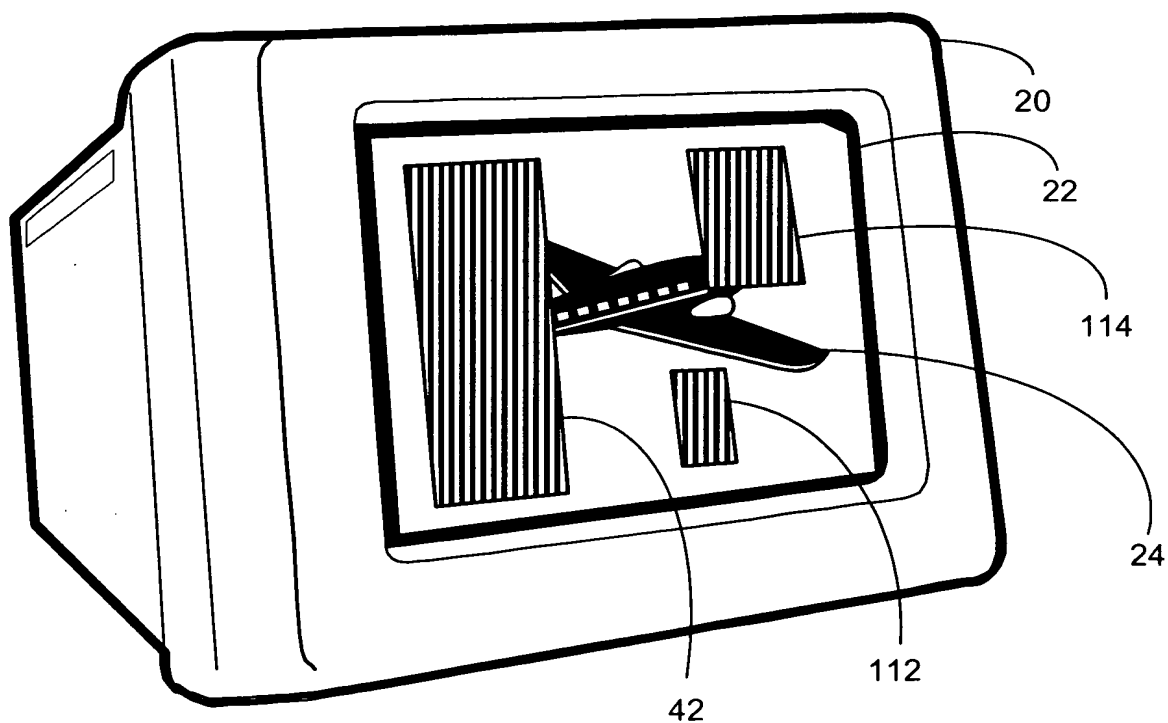


FIG. 4

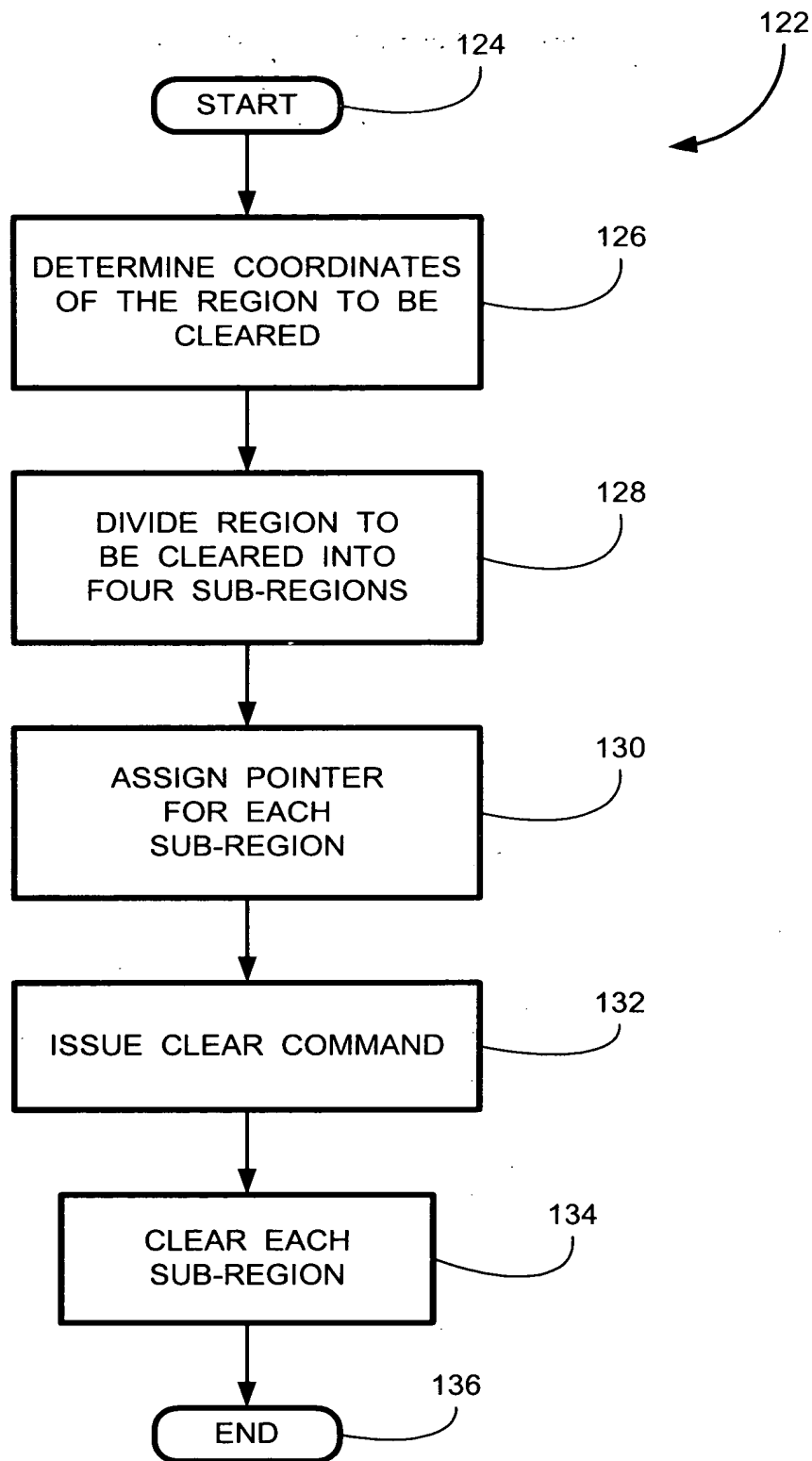
FRAME BUFFER MEMORY  
REGION 102

The diagram illustrates a frame buffer memory layout. It features a grid of memory cells. The top portion is divided into two sub-regions, C and D, each containing a vertical column of dots representing pixel data. Below these is an unaligned bottom portion. The entire structure is labeled as frame buffer memory 74, and the pixel data is labeled as pixel data 28.

**FIG. 6**



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**FIG. 8**